REMARKS

Claims 15-28 are pending in the present application. Claims 15-20, 22 and 29 were amended in this response. No new matter has been introduced as a result of the amendments. Favorable reconsideration is respectfully requested. The substantive portions of this paper are the same as the Response filed January 20, 2006, and the additional remarks are directed to the items deemed non-compliant.

The drawings were objected to for informalities. In light of the present amendments to the drawings and specification, Applicant submits the objectionable matter has been addressed. No new matter has been introduced as a result of the amendments. Withdrawal of the objection is earnestly requested. With regard to the drawings, Applicant has attached an annotated sheet showing the changes that were made in the drawing. The following references were changed from AT, ET (T1); AT ET (T2); ES (STRG), AR1-4 (PLL_WORD) and AT to AT1, ET1 (T1), AT2, ET2 (T2), ESG (STRG), A1-4 (PLL_WORD) and ATP, respectively.

The specification was also objected to for informalities. In light of the present amendments, applicants submit the objectionable matter has been addressed. Applicant has also presented amendments to the Abstract on a separate page, per the Examiner's request. No new matter has been introduced as a result of the amendments. With regard to the originally amended specification, Applicant notes that the specification begins on page 1, and that a title was provided (see bottom of page 1). As such, Applicant respectfully submits that the amended specification, including the present amendments, conform with 37 C.F.R. §1.125. Withdrawal of the objection is earnestly requested

The claims were objected to for informalities. In light of the presently submitted amendments, Applicants submit the objectionable matter has been addressed. With regard to the term "at least one control device," Applicant notes that the term, when fully read, recites "the control device control information items" which has antecedent basis. Withdrawal of the objections are earnestly requested.

Claims 15-28 were rejected under 35 U.S.C. §112, second paragraph as being indefinite. In light of the present amendments, Applicant submits the rejection is traversed. Regarding the issue surrounding the sampling via a phase-locked loop, Applicant notes that the recited claims are directed towards automatically generating a clock signal for scanning data signals, where a

data signal is scanned successively with clock signals having a different frequency given the acquisition of the clock signal during the synchronization process. Further support may be found in the specification on pages 11 and 12 (Automatic Operating Mode). As an example, a number of different clock signals are already stored in the phase/frequency control loop PLL prior to the reception of user data or data signals. These stored clock signals represent expected transmission protocols, having corresponding transmission protocol-specific frequencies, that are transmitted with the assistance of the data signals. Accordingly, the stored clock signals are adjusted for the scanning of the received data signals corresponding to the expected transmission protocols. Corresponding protocol-specific protocol identification information is allocated to each transmission protocol, and the bits of control loop information stored in the memory MEM are cyclically read out during. Withdrawal of the rejection is earnestly requested.

Claims 15-21 and 23-28 were rejected under 35 U.S.C §102(e) as being anticipated by *Van Court* (US Patent 5,917,552). Claim 22 was indicated as containing allowable subject matter. Applicant respectfully traverse this ejection.

Specifically, *Van Court* fails to teach or suggest the features of "sampling, during a synchronization process, a data signal successively using a clock signal at different frequencies which are associated with different transmission protocols; and checking the data signal, during a synchronization process, for the presence of protocol identification information associated with a selected clock signal until the protocol identification information is detected" as recited in claim 15 and similarly recited in claim 19.

Van Court teaches a PLL circuit (Figure 3a) for generating a clock signal for clock recovery where the clock signal VCOCLK is divided and individually processed at comparator 220 to achieve synchronization (col. 10, lines 4-39). However, *Van Court* fails to teach scanning the data signal successively with clock signals having different frequencies during a synchronization process and checking with respect to the presence of protocol identification information, which is allocated to the current clock signal, until a protocol identification information is detected in the scanned data stream. *Van Court* detects actively determined protocol parameters of an incoming video signal (see table 2 in column 13) and the incoming video signal is correspondingly further processed dependent on the detected result (see abstract).

This is materially different from the presently recited claims, since neither video protocol parameters are processed nor do active measurements occur at an incoming data signal.

In light of the above, Applicant respectfully submits that the rejection under 35 U.S.C. §102 is improper and should be withdrawn. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any additional fees are due in connection with this application as a whole, the Examiner is authorized to deduct such fees from deposit account no. 02-1818. If such a deduction is made, please indicate the attorney docket no. (0112740-321) on the account statement.

Respectfully submitted,

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